APPLICATION

FOR

UNITED STATES LETTERS PATENT

TITLE: THIN-FILM PHOTOELECTRIC CONVERSION DEVICE AND A METHOD OF MANUFACTURING THE SAME

APPLICANT: SHUNPEI YAMAZAKI AND YASUYUKI ARAI

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Date of Deposit 3-27-96

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Stefanie Greenamyer

PATENT

ATTORNEY DOCKET NO. 07977/023002

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Shunpei Yamazaki et al. Art Unit: 1109

Parent Serial No.: 08/623,336 Examiner: A. Weisstuch

Parent Filed : 3/27/96

Title : THIN-FILM PHOTOELECTRIC CONVERSION DEVICE AND A METHOD OF MANUFACTURING THE SAME

Assistant Commissioner for Patents
Washington, DC 20231

REQUEST FOR FILING CONTINUATION/DIVISIONAL APPLICATION

This is a request for filing a divisional application under 37 CFR 1.60, of pending prior application Serial No. 08/623,336 filed on March 27, 1996 by Shunpei Yamazaki and Yasuyuki Arai for THIN-FILM PHOTOELECTRIC CONVERSION DEVICE AND A METHOD OF MANUFACTURING THE SAME.

1. Enclosed is a true copy of the above identified prior application, including the declaration as originally filed including any amendments referred to therein, none of which introduced new matter. The true copy of the prior application is as follows: 26 page(s) of specification; 5 page(s) of claims; 1

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page(s) of abstract; 4 sheet(s) of drawings; and 2 page(s) of declaration and power of attorney.

2. Cancel in this application claims 2-25 of the prior application before calculating the filing fee. At least one original independent claim has been retained for the purpose of filing this application.

3. A preliminary amendment is enclosed. Claims added by this amendment have been properly numbered consecutively beginning with the number next following the highest numbered original claim in the prior application.

4. A substitute specification, as filed in the parent case is enclosed. Please enter this amendment prior to examination.

5. The filing fee, based on the original claims in the prior application less any claims canceled herein, is calculated below:

CLAIMS AS FILED	Number Filed		Number Extra		Rate		Basic Fee
							$770
Total Claims	[1]	- 20 =	[0]	x	$ 22	=	[-0-]
Independent Claims	[1]	- 3 =	[0]	x	$ 80	=	[-0-]
Multiple Dependent Claims					$260	=	[-0-]
				Total Filing Fee		=	[770]

6. Enclosed are 4 sheet(s) of formal drawings for use in this application.

7. Priority of Japanese applications:

serial number 7-129865 filed on March 27, 1995;

serial number 7-12984 filed on March 27, 1995; and

serial number 7-110121 filed on April 11, 1995 is claimed under 35 U.S.C. 119.

The certified copies have been filed in prior U.S. application serial number 08/623,336 filed on March 27, 1996.

8. Priority of U.S. application serial number 08/623,336 filed March 27, 1995 is claimed under 35 U.S.C. §120.

9. Please amend the specification by inserting before the first line the sentence: --This is a divisional of copending application Serial No. 08/623,336, filed March 27, 1995.--

10. With respect to the prior application from which this application claims benefit under 35 U.S.C. 120, the inventors named in this application are the same.

11. The prior application is assigned of record to Semiconductor Energy Laboratory Co., Ltd., a Japanese corporation, by virtue of an assignment submitted to the Patent and Trademark Office for recording on March 27, 1996 at REEL 7968/FRAME 0452.

12. The fees for claims remaining after the Preliminary Amendment are calculated below:

CLAIMS AS FILED	Number Filed		Number Extra		Rate		Basic Fee
							$-0-
Total Claims	[55]	- 20 =	[35]	x	$ 22	=	[770]
Independent Claims	[7]	- 3 =	[4]	x	$ 80	=	[320]
Multiple Dependent Claims					$260	=	[-0-]
				Total Filing Fee =			[1,090]

13. Two Information Disclosure Statements are being filed herewith. 1) A copy of the Information Disclosure Statement filed March 5, 1997 in case no. 08/623,336. Official consideration and citation is requested. 2) A new Information Disclosure Statement listing new documents is also being filed.

14. Enclosed is a check in the amount of $1,860.

15. The Commissioner is hereby authorized to charge any fees which may be required by this paper, or credit any overpayment, to Deposit Account No. 06-1050. A duplicate of this request is enclosed.

16. The power of attorney in the prior application is to Scott C. Harris, Reg. No. 32,030. Address all future communications to Scott C. Harris at Fish & Richardson P.C., 4225 Executive Square, Ste. 1400, La Jolla, CA 92037.

17. A petition with the required fee to extend the term in the prior application is believed unnecessary. Should any such petition be necessary, please take this paragraph as requesting that extension and charge any fees to deposit account listed in item 15.

Respectfully submitted,

Date: 8/6/97

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PATENT
ATTORNEY DOCKET NO. 07977/023002

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Shunpei Yamazaki *et al.* Art Unit: 1109

Parent
Serial No.: 08/623,336 Examiner: A. Weisstuch

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Title: THIN-FILM PHOTOELECTRIC CONVERSION DEVICE AND A METHOD OF MANUFACTURING THE SAME

Assistant Commissioner for Patents
Washington, DC 20231

PRELIMINARY AMENDMENT

Sir:

Prior to initial examination, kindly amend the application as follows.

In the Claims

Kindly cancel claim 1, and substitute the following new claims.

-- 26. A method of manufacturing a semiconductor device comprising:

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providing a semiconductor film on an insulating surface;

providing at least part of the semiconductor film with a catalyst metal containing material;

crystallizing said semiconductor film in a way that causes said catalyst metal to diffuse through the semiconductor film and function to promote a crystallization of a material of the semiconductor film;

forming a gettering layer in contact with said semiconductor film after the crystallization, said gettering layer including phosphorous; and

thermally annealing said semiconductor film and said gettering layer at a temperature not lower than 500°C in order to getter the catalyst metal in said semiconductor film using said gettering layer.

27. A method according to claim 26 wherein said semiconductor device is a photoelectric conversion device.

28. A method according to claim 26 wherein said thermally annealing is continued for 1-4 hours.

29. A method according to claim 26 wherein said gettering layer comprises a phosphorous silicate glass containing phosphorous at a concentration of 1 to 30 wt%.

30. A method according to claim 26 wherein said gettering layer comprises silicon containing phosphorous at a concentration of 0.1 to 10 wt%.

31. A method according to claim 26 wherein said thermal annealing is conducted at a temperature not higher than 800°C.

32. A method according to claim 26 wherein said catalyst metal is selected from the group consisting of Ni, Fe, Co, Ru, Rh, Pd, Os, Ir, Pt, Cu and Au.

33. A method according to claim 26 further comprising a step of removing said gettering layer after the gettering.

34. A method of manufacturing a semiconductor device comprising:

providing a substantially intrinsic semiconductor film on an insulating surface, said semiconductor film comprising silicon doped with boron at a concentration of 0.001 - 0.1 atm%;

providing at least a part of said semiconductor film with a catalyst metal-containing material;

crystallizing said semiconductor film in a way that causes said catalyst metal to diffuse through the semiconductor film and functions to promote a crystallization of said semiconductor film;

forming a gettering layer in contact with said semiconductor film after the crystallization, said gettering layer including phosphorous; and

thermally annealing said semiconductor film and said gettering layer in order to getter the catalyst metal in said semiconductor film by said gettering layer.

35. A method according to claim 34 wherein said semiconductor device is a photoelectric conversion device.

36. A method according to claim 34 wherein said thermal annealing is continued for 1-4 hours.

37. A method according to claim 34 wherein said gettering layer comprises a phosphorous silicate glass containing phosphorous at a concentration of 1 to 30 wt%.

38. A method according to claim 34 wherein said gettering layer comprises silicon containing phosphorous at a concentration of 0.1 to 10 wt%.

39. A method according to claim 34 wherein said catalyst metal is selected from the group consisting of Ni, Fe, Co, Ru, Rh, Pd, Os, Ir, Pt, Cu and Au.

40. A method according to claim 34 further comprising a step of removing said gettering layer after the gettering.

41. A method according to claim 34 wherein said thermal annealing is conducted within a temperature from 500°C to 800°C.

42. A method of manufacturing a semiconductor device comprising:

providing a semiconductor film on an insulating surface;

providing a catalyst metal-containing material on at least part of said semiconductor film;

crystallizing said semiconductor film in a way that causes said catalyst metal to diffuse through the semiconductor film and function to promote a crystallization of said semiconductor film;

forming a gettering layer in contact with said semiconductor film after the crystallization, said gettering layer including phosphorous; and

thermally annealing said semiconductor film and said gettering layer in a nitrogen atmosphere in order to getter the catalyst metal contained in said semiconductor film by said gettering layer.

43. A method according to claim 42 wherein said semiconductor device is a photoelectric conversion device.

44. A method according to claim 42 wherein said thermal annealing is continued for 1-4 hours.

45. A method according to claim 42 wherein said gettering layer comprises a phosphorous silicate glass containing phosphorous at a concentration of 1 to 30 wt%.

46. A method according to claim 42 wherein said gettering layer comprises silicon containing phosphorous at a concentration of 0.1 to 10 wt%.

47. A method according to claim 42 wherein said semiconductor film comprises silicon.

48. A method according to claim 42 wherein said catalyst metal is selected from the group consisting of Ni, Fe, Co, Ru, Rh, Pd, Os, Ir, Pt, Cu and Au.

49. A method according to claim 42 further comprising a step of removing said gettering layer after the gettering.

50. A method according to claim 42 wherein said thermal annealing is conducted within a temperature from 500°C to 800°C.

51. A method of manufacturing a semiconductor device having a intrinsic to doped junction, said method comprising:

providing a semiconductor film comprising amorphous silicon on an insulating surface;

providing a catalyst metal-containing material on at least part of said semiconductor film;

crystallizing said semiconductor film by heating in a way that causes said metal to diffuse through the semiconductor film and to promote a crystallization thereof;

forming a gettering layer in contact with said semiconductor film after the crystallization;

thermally annealing said semiconductor film and said gettering layer at a temperature not lower than 500°C in order to getter the metal included in said semiconductor film by said gettering layer; and

forming a doped silicon film on said semiconductor film to form an intrinsic to doped junction.

52. A method according to claim 51 wherein said semiconductor device is a photoelectric conversion device.

53. A method according to claim 51 wherein said thermally annealing is continued for 1-4 hours.

54. A method according to claim 51 wherein said gettering layer comprises a phosphorous silicate glass containing phosphorous at a concentration of 1 to 30 wt%.

55. A method according to claim 51 wherein said gettering layer comprises silicon containing phosphorous at a concentration of 0.1 to 10 wt%.

56. A method according to claim 51 wherein said thermal annealing is conducted at a temperature not higher than 800°C.

57. A method according to claim 51 wherein said catalyst metal is selected from the group consisting of Ni, Fe, Co, Ru, Rh, Pd, Os, Ir, Pt, Cu and Au.

58. A method according to claim 51 further comprising a step of removing said gettering layer after the gettering.

59. A method of manufacturing a semiconductor device having a doped to intrinsic junction, said method comprising:

providing a substantially intrinsic semiconductor film on an insulating surface, said semiconductor film comprising amorphous silicon doped with boron at a concentration of 0.0001 - 0.1 atm%;

providing a catalyst metal at least partly on said semiconductor material;

crystallizing said semiconductor film by heating to cause said catalyst metal to diffuse through the semiconductor film and to promote a crystallization of said semiconductor film;

forming a gettering layer in contact with said semiconductor film after the crystallization thereof;

thermally annealing said semiconductor film and said gettering layer in order to getter the catalyst metal in said semiconductor film by said gettering layer; and

forming a doped to intrinsic junction using said intrinsic semiconductor film.

60. A method according to claim 59 wherein said semiconductor device is a photoelectric conversion device.

61. A method according to claim 59 wherein said thermal annealing is continued for 1-4 hours.

62. A method according to claim 59 wherein said gettering layer comprises a phosphorous silicate glass containing phosphorous at a concentration of 1 to 30 wt%.

63. A method according to claim 59 wherein said gettering layer comprises silicon containing phosphorous at a concentration of 0.1 to 10 wt%.

64. A method according to claim 59 wherein said catalyst metal is selected from the group consisting of Ni, Fe, Co, Ru, Rh, Pd, Os, Ir, Pt, Cu and Au.

65. A method according to claim 59 further comprising a step of removing said gettering layer after the gettering.

66. A method according to claim 59 wherein said thermal annealing is conducted within a temperature from 500°C to 800°C.

67. A method of manufacturing a semiconductor device having a doped to intrinsic junction, said method comprising:

providing a semiconductor film comprising amorphous silicon formed on an insulating surface;

providing a catalyst metal-containing material at least partly on said semiconductor film;

crystallizing said semiconductor film by heating in a way that causes said catalyst metal to diffuse through the semiconductor film and function to promote the crystallization of said semiconductor film;

forming a gettering layer in contact with said semiconductor film after the crystallization; and

thermally annealing said semiconductor film and said gettering layer in a nitrogen atmosphere in order to getter the catalyst metal contained in said semiconductor film by said gettering layer; and

forming an intrinsic-to-doped junction on said semiconductor film.

68. A method according to claim 67 wherein said semiconductor device is a photoelectric conversion device.

69. A method according to claim 67 wherein said thermal annealing is continued for 1-4 hours.

70. A method according to claim 67 wherein said gettering layer comprises a phosphorous silicate glass containing phosphorous at a concentration of 1 to 30 wt%.

71. A method according to claim 67 wherein said gettering layer comprises silicon containing phosphorous at a concentration of 0.1 to 10 wt%.

72. A method according to claim 67 wherein said semiconductor film comprises silicon.

73. A method according to claim 67 wherein said catalyst metal is selected from the group consisting of Ni, Fe, Co, Ru, Rh, Pd, Os, Ir, Pt, Cu and Au.

74. A method according to claim 67 further comprising a step of removing said gettering layer after the gettering.

75. A method according to claim 67 wherein said thermal annealing is conducted within a temperature from 500°C to 800°C.

76. A method of manufacturing a semiconductor device, comprising:

providing a semiconductor film on a substrate;

forming a catalyst metal-containing material, said catalyst being a material which facilitates crystallization of said semiconductor film to be formed more easily, but which when present in a final product of the semiconductor device will degrade operation of the semiconductor device;

crystallizing said semiconductor film in a way that causes said catalyst metal-containing material to diffuse into at

least a part of the semiconductor film, said catalyst metal containing material when so diffused functioning to facilitate said crystallization;

forming a further processing layer in contact with said semiconductor film, said further processing layer including a material that reduces a concentration of said catalyst metal-containing material; and

processing said semiconductor film and said further processing layer to reduce a concentration of said catalyst metal in said semiconductor film.

77. A method as in claim 76, wherein said further processing layer includes phosphorous.

78. A method as in claim 76, wherein said metal includes Nickel.

79. A method as in claim 76, wherein said catalyst material allows said crystallization to occur at a lower temperature.

80. A method as in claim 76, wherein said further processing layer is a gettering layer. --

REMARKS

Consideration of these new claims is requested.

If there are any other charges, or any credits, please apply them to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 8/6/97

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THIN-FILM PHOTOELECTRIC CONVERSION DEVICE AND A METHOD OF MANUFACTURING THE SAME

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a thin-film photoelectric conversion device, especially a solar cell which is formed on a substrate, and more particularly to a thin-film solar cell having a photoelectric conversion layer formed of a crystalline silicon film.

2. Description of the Related Art

A solar cell or a solar battery can be manufactured using a variety of semiconductor materials or organic compound materials. However, from the industrial viewpoint, silicon which is of a semiconductor is mainly used for the solar cell. The solar cells using silicon can be classified into a bulk solar cell using a wafer of monocrystal silicon or polycrystal silicon and a thin-film solar cell having a silicon film formed on a substrate. The reduction of manufacture costs is required, and the thin-film solar cell is expected in the effect of reducing the costs because raw materials are less used for the thin-film solar cell than that for the bulk solar cell.

In the field of thin-film solar cell, an amorphous silicon solar cell has been put into practical use. However, since the amorphous silicon solar cell is lower in conversion efficiency compared with the

monocrystal silicon or polycrystal silicon solar cell and also suffers from problems such as the deterioration due to light and so on, the use thereof is limited. For that reason, as another means, a thin-film solar cell using a crystalline silicon film has been also developed.

A melt recrystallization method and a solid-phase growth method are used for obtaining a crystalline silicon film in the thin-film solar cell. Both the methods are that an amorphous silicon is formed on a substrate and recrystallized, thereby obtaining a crystalline silicon film. In any event, the substrate is required to withstand the crystallization temperature, whereby usable material is limited. In particular, in the melt recrystallization method, the substrate has been limited to a material that withstands 1,412°C, which is the melting point of silicon.

The solid-phase growth method is of a method in which an amorphous silicon film is formed on the substrate and crystallized thereafter through a heat treatment. In such a solid-phase growth method, in general, as the temperature becomes high, the processing time may be shortened more. However, the amorphous silicon film has been hardly crystallized at a temperature of 500°C or lower. For example, when the amorphous silicon film which has been grown through a gas-phase growth method is heated at 600°C so as to be crystallized, 10 hours are required. Also, when the heat treatment is conducted at the temperature of 550°C, a 100 hour or longer is required for the heat treatment.

For the above reason, a high heat resistance has been required for the substrate of the thin-film solar cell. Therefore, glass, carbon or ceramic was used for the substrate. However, from the viewpoint of reducing the costs of the solar cell, those substrates are not always proper, and it has been desired that the solar cell is fabricated on a substrate which is most generally used and inexpensive. However, for example, the #7059 glass substrate made by Corning, which is generally used, has a strain point of 593°C, and the conventional crystallization technique allows the substrate to be strained and largely deformed. For that reason, such a substrate could not be used. Also, since a substrate made of a material essentially different from silicon is used, monocrystal cannot be obtained even through crystallization is conducted on the amorphous silicon film through the above means, and silicon having large crystal grains is hard to obtain. Consequently, this causes a limit to an improvement in the efficiency of the solar cell.

In order to solve the above problems, a method of crystallizing an amorphous silicon film through a heat treatment is disclosed in U.S. Patent 5,403,772. According to the method disclosed in this patent, in order to accelerate crystallization at a low temperature, a small amount of metal elements are added to the amorphous silicon film as a catalyst material. Further, there is disclosed that the lowering of a heat treatment temperature and the reduction of a treatment time are enabled. Also, there is disclosed in the publication that a simple

substance of nickel (Ni), iron (Fe), cobalt (Co) or platinum (Pt), or a compound of any one of those materials and silicon, or the like is suitable for the catalyst material.

However, since any catalyst material used for accelerating crystallization is a material which is naturally undesirable for crystalline silicon, it has been desired that the concentration of the catalyst material is as low as possible. The concentration of a catalyst material necessary for accelerating crystallization was $1 \times 10^{17}/cm^3$ to $1 \times 10^{20}/cm^3$. However, even when the concentration is relatively low, since the above catalyst material is a heavy metal element, the material contained in silicon forms a defect level, thereby lowering the characteristic of a fabricated element.

By the way, the principle of operation of a solar cell fabricated by forming a p-n junction can be roughly described as follows. The solar cell absorbs light and generates the charges of electrons/holes due to an absorbed light energy. The electrons move toward an n-layer side, and the holes move toward a p-layer side due to the drifts caused by a junction electric field and diffusion. However, when the defect level are high in silicon, the charges are trapped by the defect level while they are moving in the silicon, thereby disappearing. In other words, the photoelectric conversion characteristics are caused to lower. A period of time since the electrons/holes generate until they disappear is called "a life time". In the solar cell, it is desirable that the lifetime is long.

Hence. it has been necessary to reduce the heavy metal elements that generate the defect level in silicon as much as possible.

SUMMARY OF THE INVENTION

The present invention has been made in view of the above circumstances, and therefore an object of the present invention is to provide a method of manufacturing a thin-film solar cell, which keeps the feature of crystallization due to the above catalyst material and removes the catalyst material after the crystallization has been completed.

Another object of the present invention is to provide a solar cell which is excellent in the photoelectric conversion characteristic, using the above method.

In accordance with the primary feature of the present invention, a method of manufacturing a photoelectric conversion device includes a step of forming a gettering layer on a crystallized semiconductor layer obtained by using the catalyst metal such as nickel. The gettering layer may be either insulative or semiconductive and contains phosphorus to absorb the eatalyst metal such as nickel from the semiconductor layer after it is crystallized, thereby, reducing the concentration of the catalyst metal in the semiconductor layer. Specifically, the method includes the steps of:

disposing a metal containing layer in contact with an upper or lower surface of a non-single crystalline silicon semiconductor layer;

crystallizing the non-single crystalline silicon semiconductor layer by heating wherein the metal functions to promote the crystallization;

forming a gettering layer on or within said semiconductor layer after crystallized, the gettering layer containing phosphorus; and

heating said semiconductor layer and the gettering layer in order to getter the metal contained in the semiconductor layer.

As the metal element, it is possible to use one or more elements of Ni, Fe, Co, Ru, Rh, Pd, Os, Ir, Pt, Cu and Au.

In accordance with a preferred embodiment of the invention, the gettering layer may be a silicon layer to which phosphorus is added during the deposition thereof onto the crystallized semiconductor layer. In an alternative, the gettering layer may be a phosphorus doped region formed within the crystallized semiconductor layer, namely, a method of the present invention includes a step of introducing ions of phosphorus into a surface region of the crystallized semiconductor layer by ion doping after crystallizing the semiconductor layer by the use of the catalyst metal. In a further alternative, the gettering layer may be a phosphorus silicate glass (PSG) layer deposited on the crystallized semiconductor layer.

In accordance with another aspect of the invention, the catalyst metal is provided by disposing the metal containing layer in contact with an upper or lower surface of a non-single crystalline semiconductor

layer to be crystallized. In the case of disposing the metal containing layer under the non-single crystalline semiconductor layer, the metal containing layer may be used also as a lower electrode of the photoelectric conversion device.

In accordance with a still another aspect of the invention, a solar cell comprises a substrate, a first crystalline silicon film having a substantially intrinsic conductivity type formed on the substrate, and a second crystalline silicon film having one conductivity type adjacent to the first crystalline silicon film, wherein the first crystalline silicon film contains a catalyst element for promoting crystallization of silicon at a concentration not higher than 5×10^{18} atoms/cm^3. The concentration value disclosed in the present invention is determined by a secondary ion mass spectroscopy and corresponds to a maximum value of the measured values.

In accordance with a further aspect of the invention, in the above mentioned solar cell, a concentration of the catalyst contained in the second crystalline silicon film is higher than the concentration of the catalyst contained in the first crystalline silicon film.

In accordance with a still further aspect of the invention, the crystalline semiconductor film obtained by using the catalyst metal such as nickel has a plurality of crystal grains in the form of needles.

According to the present invention, the lifetime of carriers in the crystalline silicon film is increased, and the excellent characteristics of the thin-film solar cell are obtained.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects and features of the present invention will be more apparent from the following description taken in conjunction with the accompanying drawings.

Figs. 1A to 1D are schematic diagrams showing a method of manufacturing a thin-film solar cell in accordance with the present invention;

Figs. 2A to 2D are schematic diagrams showing a method of manufacturing a thin-film solar cell in accordance with the present invention;

Fig. 3 is a diagram showing one example of a cross-sectional structure of a thin-film solar cell in accordance with the present invention; and

Fig. 4 is a diagram showing one example of a cross-sectional structure of a thin-film solar cell in accordance with the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Now, a description will be given in more detail of embodiments of the present invention with reference to the accompanying drawings.

(First Embodiment)

A first embodiment shows a process of manufacturing a thin-film solar cell which is manufactured through a method of forming an amorphous silicon film in close contact with metal elements that accelerate the crystallization of silicon, crystallizing said amorphous silicon film through a heat treatment, and removing said metal elements remaining in the amorphous silicon film after the crystallization.

This embodiment will be described with reference to Figs. 1A to 1D. In this embodiment, nickel is used as metal elements having a catalyst action that accelerates the crystallization of silicon. First, a silicon oxide film 102 having a thickness of 0.3 μm is formed on a glass substrate (for example, Corning 7059 glass substrate) 101 as an underlying layer. The silicon oxide film 102 is formed through a plasma CVD technique with a raw material of tetra ethoxy silane (TEOS), and also can be formed through a sputtering technique as another method. Subsequently, an amorphous silicon film 103 is formed with a raw material of silane gas through a plasma CVD technique. The formation of the amorphous silicon film 103 may be conducted using a low pressure thermal CVD technique, a sputtering technique or an evaporation method. The above amorphous silicon film 103 may be a substantially-intrinsic amorphous silicon film or may contain boron (B) at 0.001 to 0.1

atms%. Also, the thickness of the amorphous silicon film 103 is set to 10 μm. It is needless to say that the thickness may be set to a required one (Fig. 1A).

Subsequently, the substrate is immersed in an ammonium hydroxide, hydrogen peroxide mixture and then held at 70°C for 5 minutes, to thereby form an oxide film (not shown) on the surface of the amorphous silicon film 103. The silicon oxide film is formed in order to improve its wettability in a process of coating nickel acetate solution which will be conducted later. Furthermore, the nickel acetate solution is coated on the surface of the amorphous silicon film 103 by spin coating. The nickel element functions as an element that accelerates the crystallization in crystallizing the amorphous silicon film 103.

Subsequently, the amorphous silicon film 103 is held at a temperature of 450°C for one hour in a nitrogen atmosphere, thereby eliminating hydrogen from the amorphous silicon film 103. This is because dangling bonds are intentionally produced in the amorphous silicon film, to thereby lower a threshold energy in crystallizing later. Then, the amorphous silicon film 103 is subjected to a heat treatment at 550°C for 4 to 8 hours in the nitrogen atmosphere, to thereby crystallize the amorphous silicon film 103. A temperature in crystallizing can be set to 550°C because of the action of nickel elements. Hydrogen of 0.001 atms% to 5 atms% is contained in a crystalline silicon film 104 which has been crystallized. During the above heat treatment, nickel element

accelerates the crystallization of the crystalline silicon film while it is moving in the silicon film.

In this way, the crystalline silicon film 104 is formed on the glass substrate. Subsequently, a phosphorus silicate glass (PSG) 105 is formed on the crystalline silicon film 104. The phosphorus silicate glass (PSG) 105 is formed, using a mixture gas consisting of silane, phosphine and oxygen, at a temperature of 450°C through an atmospheric CVD technique. The concentration of phosphorus in the phosphorus silicate glass is set to 1 to 30 wt%, preferably 7 wt%. The phosphorus silicate glass (PSG) 105 is to getter nickel remaining in the crystalline silicon film. Even though the phosphorus silicate glass 105 is merely formed at 450°C, its effect is obtained. More effectively, the phosphorus silicate glass 105 may be subjected to a heat treatment at a heat treatment temperature of 500 to 800°C, preferably 550°C for 1 to 4 hours in the nitrogen atmosphere. As another method, the phosphorus silicate glass 105 can be replaced by a silicon film to which phosphorus of 0.1 to 10 wt% has been added with the same effect (Fig. 1B).

Thereafter, the phosphorus silicate glass 105 is etched using a hydrogen fluoride aqueous solution so as to be removed from the surface of the crystalline silicon film 104. As a result, the surface of the crystalline silicon film 104 is exposed from the main surface of the substrate 101. On that surface is formed an n-type crystalline silicon film 106. The n-type crystalline silicon film 106 may be formed

through a plasma CVD technique or through a low pressure thermal CVD technique. The n-type crystalline silicon film 106 is desirably formed at a thickness of 0.02 to 0.2 μm, and in this embodiment, it is formed at a thickness of 0.1 μm (Fig. 1C).

Then, a transparent electrode 107 is formed on the above n-type crystalline silicon film 106. The transparent electrode 107 is made of indium tin oxide alloy (ITO) and has a thickness of 0.08 μm through a sputtering technique. Finally, a process of providing lead electrodes 108 is conducted. In providing the lead electrodes 108, as shown in Fig. 1D, a minus side electrode is disposed on the transparent electrode 107, and a plus side electrode is disposed on the crystalline silicon film 104 by removing parts of the transparent electrode 107, the n-type crystalline silicon film 106 and the crystalline silicon film 104. The lead electrodes 108 can be formed by sputtering or vacuum evaporation, or using aluminum, silver, silver paste or the like. Furthermore, after the provision of the lead electrodes 108, the product is subjected to a heat treatment at 150°C to 300°C for several minutes with the result that the adhesion between the lead electrodes 108 and the underlying layer becomes high, thereby obtaining an excellent electric characteristic. In this embodiment, the product is subjected to a heat treatment at 200°C for 30 minutes in a nitrogen atmosphere using an oven.

Through the above-mentioned processes, a thin-film solar cell is completed.

(Second Embodiment)

In a second embodiment, there is shown a thin-film solar cell which was formed in the process where a metal element that accelerates the crystallization of crystalline silicon is removed after crystallization through the method where phosphorus is implanted through a plasma doping method into the surface of crystalline silicon film.

A second embodiment will be described with reference to Figs. 2A to 2D. Nickel is used to accelerate the crystallization of silicon as a metal element working as a catalyst in this embodiment. First, a silicon oxide film 202 having a thickness of 0.3 μm is formed on a glass substrate (for example, Corning 7059 glass substrate) 201 as an underlying layer. The silicon oxide film 202 is formed by plasma CVD with a raw material of tetra ethoxy silane (TEOS), and also can be formed through a sputtering technique as another method. Subsequently, an amorphous silicon film 203 is formed with a raw material of silane gas through a plasma CVD technique. The formation of the amorphous silicon film 203 may be conducted using a low pressure thermal CVD technique, a sputtering technique or an evaporation method. The above amorphous silicon film 203 may be a substantially-intrinsic amorphous silicon film or an amorphous silicon film to which boron (B) of 0.001 to 0.1 atms% has been added. Also, the thickness of the amorphous silicon film 203 is set to 20 μm. It is needless to say that the thickness may be set to a required one (Fig. 2A).

Thereafter, the substrate is immersed in an ammonium hydroxide. hydrogen peroxide mixture at 70°C for 5 minutes, to thereby form an oxide film (not shown) on the surface of the amorphous silicon film 203. The silicon oxide film is formed in order to improve its wettability in a process of coating nickel acetate solution which will be conducted later. Furthermore, the nickel acetate solution is coated on the surface of the amorphous silicon film 203 by spin coating. The nickel element functions as an element that accelerates the crystallization in crystallizing the amorphous silicon film 203.

Subsequently, the amorphous silicon film 203 is held at a temperature of 450°C for one hour in a nitrogen atmosphere, thereby eliminating hydrogen from the amorphous silicon film 203. This is because dangling bonds are intentionally produced in the amorphous silicon film, to thereby lower a threshold energy in crystallizing later. Then, the amorphous silicon film 203 is subjected to a heat treatment at 550°C for 4 to 8 hours in a nitrogen atmosphere, to thereby crystallize the amorphous silicon film 203. A temperature in crystallizing can be set to 550°C because of the action of nickel elements. Hydrogen of 0.001 atms% to 5 atms% is contained in a crystalline silicon film 204 which has been crystallized. During the above heat treatment, nickel elements accelerates the crystallization of the crystalline silicon film 204 while it is moving in the silicon film.

In this way, the crystalline silicon film 204 can be formed on the glass substrate. In this state, the implantation of phosphorus (P) ions is conducted by a plasma doping method. The dose amount may be set to 1 x 10^{14} to 1 x $10^{17}/cm^2$, and in this embodiment, it is set to 1 x $10^{16}/cm^2$. An accelerating voltage is set to 20 keV. Through this process, a layer containing phosphorus with a high concentration therein is formed within a region of 0.1 to 0.2 μm depthwise from the surface of the crystalline silicon film 204. Thereafter, a heat treatment is conducted on the crystalline silicon film 204 in order to getter nickel remaining in the crystalline silicon film 204. The crystalline silicon film 204 may be subjected to a heat treatment at 500 to 800°C, preferably 550°C for 1 to 4 hours in the nitrogen atmosphere (Fig. 2B).

In the crystalline silicon film 204, since a region into which phosphorus ions have been implanted has crystal destroyed, it becomes of a substantially amorphous structure immediately after the ions have been implanted thereinto. Thereafter, since that region is crystallized through said heat treatment, it is usable as the n-type layer of the solar cell even in this state. In this case, the concentration of nickel in the i-type or p-type layer 204 is lower than in the phosphorus doped n-type layer.

In accordance with the preferred embodiment of the invention, the phosphorus doped region is more desirably removed since nickel that has functioned as a catalyst element is segregated in this region. As

the removing method, after a natural oxide film thinly formed on the surface has been etched using a hydrogen fluoride aqueous solution, it is removed using sulfur hexafluoride and nitric trifluoride through by dry etching. With this process, the surface of the crystalline silicon film 204 is exposed. On that surface is formed an n-type crystalline silicon film 205. The n-type crystalline silicon film 205 may be formed by plasma CVD or low pressure thermal CVD. The n-type crystalline silicon film 205 is desirably formed at a thickness of 0.02 to 0.2 μm, and in this embodiment, it is formed at a thickness of 0.1 μm (Fig. 2C).

Then, a transparent electrode 206 is formed on the above n-type crystalline silicon film 205. The transparent electrode 206 is made of indium tin oxide alloy (ITO) and has a thickness of 0.08 μm through a sputtering technique. Finally, a process of providing lead electrodes 207 is conducted. In providing the lead electrodes 207, as shown in Fig. 2D, a minus side electrode is disposed on the transparent electrode 206, and a plus side electrode is disposed on the crystalline silicon film 204 by removing parts of the transparent electrode 206, the n-type crystalline silicon film 205 and the crystalline silicon film 204. The lead electrodes 207 can be formed through a sputtering technique or an evaporation method, using aluminum, silver, silver paste or the like. Furthermore, after the provision of the lead electrodes 207, the substrate is subjected to a heat treatment at 150°C to 300°C for several minutes with the result that the adhesion between the lead electrodes 207 and the underlying

layer becomes high, thereby obtaining an excellent electric characteristic. In this embodiment, the substrate is subjected to a heat treatment at 200°C for 30 minutes in a nitrogen atmosphere using an oven.

Through the above-mentioned processes, a thin-film solar cell is completed.

(Third Embodiment)

A third embodiment shows an example where in the process of manufacturing the thin-film solar cell described with reference to the first and second embodiments, the surface of the crystalline silicon film is subjected to an anisotropic etching process so as to make the surface of the solar cell irregular as shown in Fig. 3. A technique by which that surface is made irregular so that the reflection from the surface of the solar cell is reduced is called "a texture technique".

A silicon oxide film 302 having a thickness of 0.3 μm is formed on a glass substrate (for example, Corning 7059 glass substrate) 301 as an underlying layer. The silicon oxide film 302 is formed by plasma CVD with a raw material of tetra ethoxy silane (TEOS), and also can be formed by sputtering as another method. Subsequently, an amorphous silicon film is formed by plasma CVD. The formation of the amorphous silicon film may be conducted by low pressure thermal CVD, sputtering, evaporation or the like. The above amorphous silicon film 303 may be a substantially-intrinsic amorphous silicon film or an amorphous silicon

film to which boron (B) of 0.001 to 0.1 atms% has been added. Also, the thickness of the amorphous silicon film is set to 20 μm. It is needless to say that the thickness may be set to a required one.

Subsequently, the substrate is immersed in an ammonium hydroxide and hydrogen peroxide mixture and then held at 70°C for 5 minutes, to thereby form an oxide film on the surface of the amorphous silicon film. The silicon film is formed in order to improve its wettability in a process of coating nickel acetate solution which will be conducted later. Furthermore, the nickel acetate solution is coated on the surface of the amorphous silicon film by spin coating. The nickel element functions as an element that accelerates the crystallization in crystallizing the amorphous silicon film.

Subsequently, the amorphous silicon film is held at a temperature of 450°C for one hour in a nitrogen atmosphere, thereby eliminating hydrogen from the amorphous silicon film. This is because unpaired couplings are intentionally produced in the amorphous silicon film, to thereby lower a threshold energy in crystallizing later. Then, the amorphous silicon film is subjected to a heat treatment at 550°C for 4 to 8 hours in the nitrogen atmosphere, to thereby crystallize the amorphous silicon film to obtain a crystalline silicon film 303. A temperature in crystallizing can be set to 550°C because of the action of nickel elements. Hydrogen of 0.001 atms% to 5 atms% is contained in the crystalline silicon film 303 which has been crystallized. During the

above heat treatment, nickel elements accelerates the crystallization of the crystalline silicon film 303 while it is moving in the silicon film.

In this way, the crystalline silicon film 303 can be formed on the glass substrate. Then, a gettering process is conducted on the crystalline silicon film 304 in order to remove nickel remaining in the crystalline silicon film 304. A method of conducting the gettering process may be a method of forming a phosphorus silicate glass (PSG) on the crystalline silicon film 303, or a method of implanting phosphorus ions into the surface of the crystalline silicon film 303.

In a method of forming the phosphorus silicate glass (PSG), the phosphorus silicate glass film is formed, using a mixture gas consisting of silane, phosphine and oxygen, at a temperature of 450°C through atmospheric CVD. The gettering process is conducted by subjecting the crystalline silicon film to a heat treatment at 550°C for 1 to 4 hours in a nitrogen atmosphere. Thereafter, the phosphorus silicate glass film is desirably etched using a hydrogen fluoride aqueous solution so as to be removed.

In the method of implanting phosphorus ions into the surface of the crystalline silicon film, the implantation of ions can be conducted through plasma doping. The dose amount may be set to 1×10^{14} to $1 \times 10^{17}/cm^2$, and in this embodiment, it is set to $1 \times 10^{16}/cm^2$. An accelerating voltage is set to 20 keV. Through this process, a layer containing phosphorus with a high concentration therein is formed

within a region of 0.1 to 0.2 μm depthwise from the surface of the crystalline silicon film. Thereafter, a heat treatment is conducted on the crystalline silicon film in order to getter nickel remaining in the crystalline silicon film. The heat treatment is conducted at a temperature of 500 to 800°C, preferably 550°C for 1 to 4 hours in the nitrogen atmosphere.

After the gettering process has been completed, the texture process is conducted on the surface of the crystalline silicon film. The texture process can be conducted using hydrazine or sodium hydroxide aqueous solution. Hereinafter, a case of using sodium hydroxide will be described.

The texture process is conducted by heating an aqueous solution containing sodium hydroxide 2% in concentration to 80°C. Under this condition, the etching rate of the crystalline silicon film thus obtained in this embodiment is about 1 μm/min. The etching is conducted for five minutes, and thereafter the crystalline silicon film is immersed in boiling water in order to immediately cease the reaction and sufficiently cleaned by flowing water. As a result of observing the surface of the crystalline silicon film which has been subjected to the texture process through an electron microscope, the unevenness of about 0.1 to 5 μm is found on the surface although it is at random.

On that surface is formed an n-type crystalline silicon film 304. The n-type crystalline silicon film 304 may be formed through a plasma

CVD technique or through a low pressure thermal CVD technique. The n-type crystalline silicon film 304 is desirably formed at a thickness of 0.02 to 0.2 μm, and in this embodiment, it is formed at a thickness of 0.1 μm.

Then, a transparent electrode 305 is formed on the above n-type crystalline silicon film 304. The transparent electrode 305 is made of indium tin oxide alloy (ITO) and has a thickness of 0.08 μm by sputtering. Finally, a process of providing lead electrodes 307 is conducted. In providing the lead electrodes 307, as shown by the structure in Fig. 3D, a minus side electrode is disposed on the transparent electrode 305, and a plus side electrode is disposed on the crystalline silicon film 303 by removing parts of the transparent electrode 305, the n-type crystalline silicon film 304 and the crystalline silicon film 303. The lead electrodes 306 can be formed by sputtering or vacuum evaporation, or using aluminum, silver, silver paste or the like. Furthermore, after the provision of the lead electrodes 307, the entire structure is subjected to a heat treatment at 150°C to 300°C for several minutes with the result that the adhesion between the lead electrodes 207 and the underlying layer becomes high, thereby obtaining an excellent electric characteristic. In this embodiment, the heat treatment was conducted at 200°C for 30 minutes in a nitrogen atmosphere using an oven.

Through the above-mentioned processes, a thin-film solar cell having the texture structure on the surface is completed.

(Fourth Embodiment)

A fourth embodiment shows a process of manufacturing a thin-film solar cell, as shown in Fig. 4, in which a coating of metal elements that accelerate the crystallization of silicon is formed on a substrate, an amorphous silicon film is formed on the coating of metal elements, and the amorphous silicon film is crystallized through a heat treatment, and after crystallization, the metal elements diffused in the silicon film are removed therefrom.

First, a coating of the metal element that accelerates the crystallization of silicon is formed on a substrate. Nickel is used as the metal element. A silicon oxide film having a thickness of 0.3 μm is first formed on a glass substrate (for example, Corning 7059 glass substrate) 401 as an underlying layer 402. The silicon oxide film is formed through a plasma CVD technique with a raw material of tetra ethoxy silane (TEOS), and also can be formed through a sputtering technique as another method. Subsequently, a nickel film 407 is formed on the substrate. The nickel film 407 having 0.1 μm is formed using a tablet made of pure nickel through an electron beam evaporation method. Then, an amorphous silicon film is formed through a plasma CVD technique. The formation of the amorphous silicon film may be conducted through low pressure thermal CVD, sputtering, evaporation or

the like. The above amorphous silicon film may be a substantially-intrinsic amorphous silicon film or an amorphous silicon film to which boron (B) of 0.001 to 0.1 atms% has been added. Also, the thickness of the amorphous silicon film is set to 10 μm. It is needless to say that the thickness may be set to a required one.

Subsequently, the amorphous silicon film is held at a temperature of 450°C for one hour in a nitrogen atmosphere, thereby eliminating hydrogen from the amorphous silicon film. This is because dangling bonds are intentionally produced in the amorphous silicon film, to thereby lower a threshold energy in crystallizing later. Then, the amorphous silicon film is subjected to a heat treatment at 550°C for 4 to 8 hours in the nitrogen atmosphere, to thereby crystallize the amorphous silicon film to obtain a crystalline silicon film 403. A temperature in crystallizing can be set to 550°C because of the action of nickel elements. Hydrogen of 0.001 atms% to 5 atms% is contained in a crystalline silicon film 403 which has been crystallized. During the above heat treatment, a small amount of nickel elements diffuse from the nickel film disposed under the amorphous silicon film into the silicon film, and accelerates the crystallization of the crystalline silicon film 403 while it is moving in the silicon film.

In this way, the crystalline silicon film 403 is formed on the glass substrate. Subsequently, a phosphorus silicate glass (PSG) is formed on the crystalline silicon film 403. The phosphorus silicate glass (PSG) is

formed, using a mixture gas consisting of silane, phosphine and oxygen, at a temperature of 450°C by atmospheric CVD. The concentration of phosphorus in the phosphorus silicate glass is set to 1 to 30 wt%, preferably 7 wt%. The phosphorus silicate glass is to getter nickel remaining in the crystalline silicon film. Even though the phosphorus silicate glass is merely formed at 450°C, its effect is obtained. More effectively, the phosphorus silicate glass may be subjected to a heat treatment at a temperature of 500 to 800°C, preferably 550°C for 1 to 4 hours in the nitrogen atmosphere. As another method, the phosphorus silicate glass can be replaced by a silicon film to which phosphorus of 0.1 to 10 wt% has been added with the same effect.

Thereafter, the phosphorus silicate glass is etched using a hydrogen fluoride aqueous solution so as to be removed from the surface of the crystalline silicon film. As a result, the surface of the crystalline silicon film 403 is exposed from the main surface of the substrate. On that surface is formed an n-type crystalline silicon film 404. The n-type crystalline silicon film 404 may be formed by plasma CVD or low pressure thermal CVD. The n-type crystalline silicon film 404 is desirably formed at a thickness of 0.02 to 0.2 μm, and in this embodiment, it is formed at a thickness of 0.1 μm.

Then, a transparent electrode 405 is formed on the above n-type crystalline silicon film 404. The transparent electrode 405 is made of indium tin oxide alloy (ITO) and has a thickness of 0.08 μm by

sputtering. Finally, a process of providing lead electrodes 406 is conducted. In providing the lead electrodes, as shown in Fig. 4, a minus side electrode is disposed on the transparent electrode 405, and a plus side electrode is disposed on the crystalline silicon film 403 by removing parts of the transparent electrode 405, the n-type crystalline silicon film 404 and the crystalline silicon film 403. The lead electrodes 406 can be formed by sputtering or vacuum evaporation, or using aluminum, silver, silver paste or the like. Furthermore, after the provision of the lead electrodes, the substrate is subjected to a heat treatment at 150°C to 300°C for example at 200°C for 30 minutes in a nitrogen atmosphere with the result that the adhesion between the lead electrodes and the underlying layer becomes high, thereby obtaining an excellent electric characteristic.

Through the above-mentioned processes, a thin-film solar cell is completed.

As was described above, in the method of manufacturing the thin-film solar cell in accordance with the present invention, in a process of crystallizing an amorphous silicon film by a heat treatment, a catalyst material such as nickel is used, thereby making it possible to obtain a crystalline silicon film at a heat treatment temperature lower than the conventional method. Furthermore, the method of the present invention enables the concentration of the catalyst material remaining in the crystalline silicon film obtained to be lowered. As a result, a thin-film

solar cell that uses an inexpensive glass substrate and is excellent in photoelectric conversion characteristic can be obtained.

The foregoing description of a preferred embodiment of the invention has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed, and modifications and variations are possible in light of the above teachings or may be acquired from practice of the invention. The embodiment was chosen and described in order to explain the principles of the invention and its practical application to enable one skilled in the art to utilize the invention in various embodiments and with various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the claims appended hereto, and their equivalents.

WHAT IS CLAIMED IS:

1. A method of manufacturing a photoelectric conversion device comprising the steps of:

disposing a metal containing layer in contact with an upper or lower surface of a non-single crystalline silicon semiconductor layer;

crystallizing said non-single crystalline silicon semiconductor layer by heating wherein said metal functions to promote the crystallization;

forming a gettering layer on or within said semiconductor layer after crystallized, said gettering layer containing phosphorus; and

heating said semiconductor layer and said gettering layer in order to getter said metal contained in said semiconductor layer.

2. The method of claim 1 wherein said metal is selected from the group consisting of Ni, Fe, Co, Ru, Rh, Pd, Os, Ir, Pt, Cu and Au.

3. The method of claim 1 wherein said photoelectric conversion device is a solar cell.

4. A method of manufacturing a photoelectric conversion device comprising the steps of:

disposing a metal containing layer in contact with a non-single crystalline silicon semiconductor layer;

crystallizing said semiconductor layer by heating wherein said metal functions to promote the crystallization thereof;

forming a phosphorus doped silicon layer on said semiconductor layer after said crystallizing; and

heating said phosphorus doped silicon layer and said semiconductor layer.

5. The method of claim 4 wherein said non-single crystalline silicon semiconductor layer is formed on a substrate having an electrode and said metal containing layer is formed on an upper surface of said semiconductor layer.

6. The method of claim 4 wherein said phosphorus doped silicon layer contains phosphorus at a concentration of 0.1 to 10 wt%.

7. The method of claim 4 further comprising a step of etching a surface of said semiconductor layer after the step of heating said phosphorus doped silicon layer and said semiconductor layer in order to make the surface of said semiconductor layer uneven.

8. The method of claim 4 wherein said photoelectric conversion device is a solar cell.

9. A method of manufacturing a photoelectric conversion device comprising the steps of:

disposing a metal containing layer in contact with a non-single crystalline silicon semiconductor layer;

crystallizing said semiconductor layer by heating wherein said metal functions to promote the crystallization thereof;

introducing phosphorus ions into a surface of said semiconductor layer after said crystallizing; and then

heating said semiconductor layer.

10. The method of claim 9 wherein said non-single crystalline silicon semiconductor layer is formed on a substrate having an electrode and said metal containing layer is formed on an upper surface of said semiconductor layer.

11. The method of claim 9 further comprising a step of etching a surface of said semiconductor layer after the step of heating said semiconductor layer in order to make the surface of said semiconductor layer uneven.

12. The method of claim 9 wherein said photoelectric conversion device is a solar cell.

13. A method of manufacturing a photoelectric conversion device comprising the steps of:

disposing a metal containing layer in contact with a non-single crystalline silicon semiconductor layer;

crystallizing said semiconductor layer by heating wherein said metal functions to promote the crystallization thereof;

forming a phosphorus silicate glass layer on said semiconductor layer after said crystallizing; and

heating said phosphorus silicate glass layer and said semiconductor layer.

14. The method of claim 13 wherein said non-single crystalline silicon semiconductor layer is formed on a substrate having an electrode and said metal containing layer is formed on an upper surface of said semiconductor layer.

15. The method of claim 13 wherein said phosphorus silicate glass layer contains phosphorus at a concentration of 1 to 30 wt%.

16. The method of claim 13 further comprising a step of etching a surface of said semiconductor layer after the step of heating said phosphorus silicate glass layer and said semiconductor layer in order to make the surface of said semiconductor layer uneven.

17. The method of claim 13 wherein said photoelectric conversion device is a solar cell.

18. A method of manufacturing a photoelectric conversion device comprising the steps of:

forming a metal layer on a substrate;

depositing a non-single crystalline silicon semiconductor layer on said metal layer;

crystallizing said semiconductor layer by heating wherein said metal functions to promote the crystallization thereof;

forming a phosphorus containing layer on or within said semiconductor layer after said crystallizing; and

heating said phosphorus containing layer and said semiconductor layer.

19. The method of claim 18 further comprising a step of etching a surface of said semiconductor layer after the step of heating said phosphorus containing layer and said semiconductor layer in order to make the surface of said semiconductor layer uneven.

20. The method of claim 18 wherein said photoelectric conversion device is a solar cell.

21. A solar cell comprising:

a substrate;

a first crystalline silicon film having a substantially intrinsic conductivity type on said substrate; and

a second crystalline silicon film having one conductivity type adjacent to said first crystalline silicon film,

wherein said first crystalline silicon film contains a catalyst element for promoting crystallization of silicon at a concentration not higher than 5×10^{18} atoms/cm^3.

22. The solar cell of claim 21 wherein said catalyst is selected from the group consisting of Ni, Fe, Co, Ru, Rh, Pd, Os, Ir, Pt, Cu and Au.

23. The solar cell of claim 21 wherein a concentration of said catalyst contained in said second crystalline silicon film is higher than said the concentration of said catalyst contained in said first crystalline silicon film.

24. The solar cell of claim 21 wherein said first crystalline silicon film has a different conductivity type than said second crystalline silicon film.

25. The solar cell of claim 21 wherein said first crystalline silicon film comprises a plurality of crystal grains in the form of needles.

ABSTRACT OF THE DISCLOSURE

A method of manufacturing a thin-film solar cell, comprising the steps of: forming an amorphous silicon film on a substrate; holding a metal element that accelerates the crystallization of silicon in contact with the surface of the amorphous silicon film; subjecting the amorphous silicon film to a heat treatment to obtain a crystalline silicon film; depositing a silicon film to which phosphorus has been added in close contact with the crystalline silicon film; and subjecting the crystalline silicon film and the silicon film to which phosphorus has been added to a heat treatment.

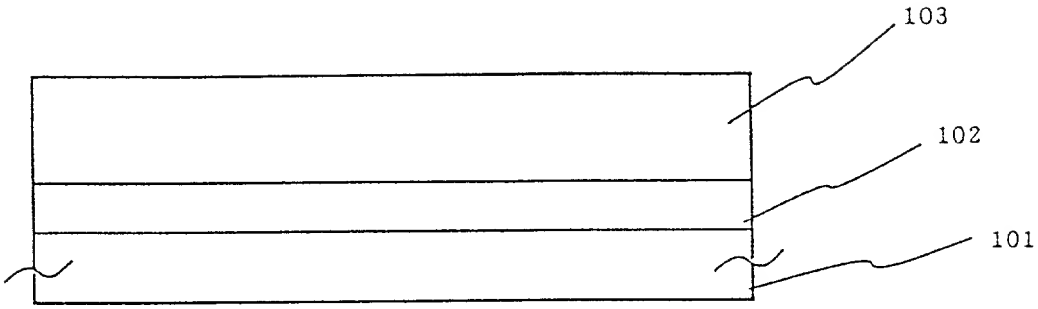


Fig. 1 (A)

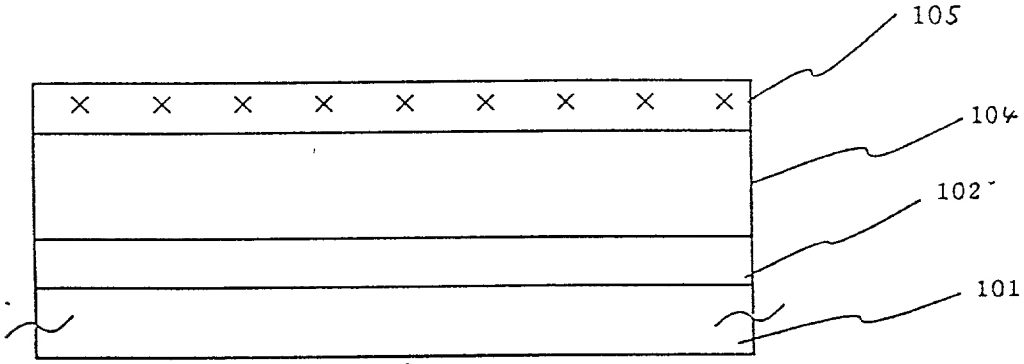


Fig. 1 (B)

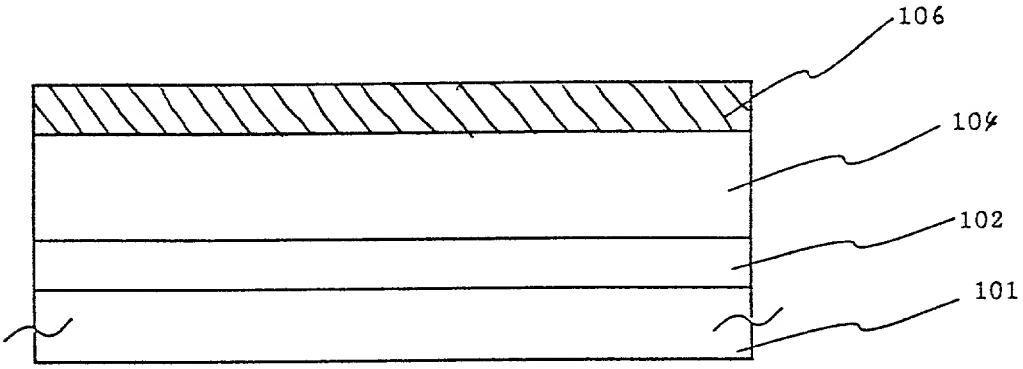


Fig. 1 (C)

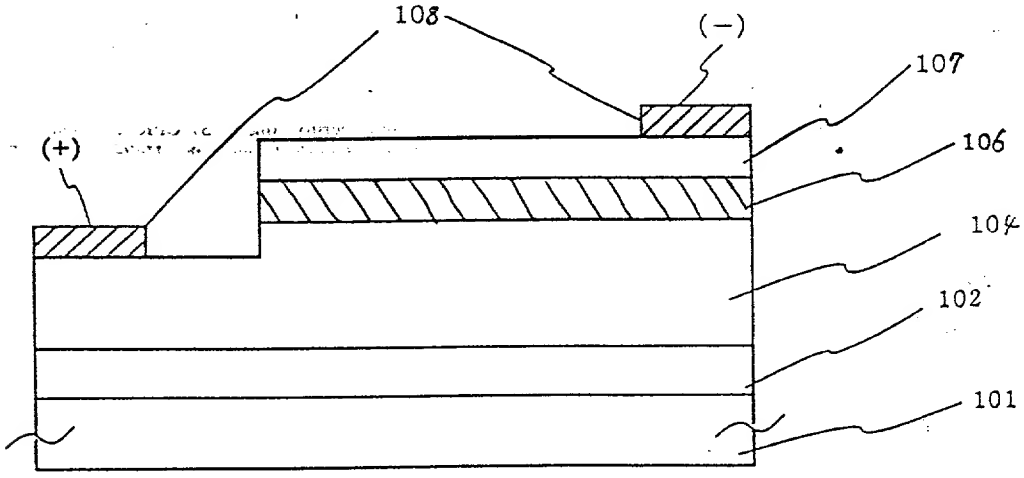


Fig. 1 (D)

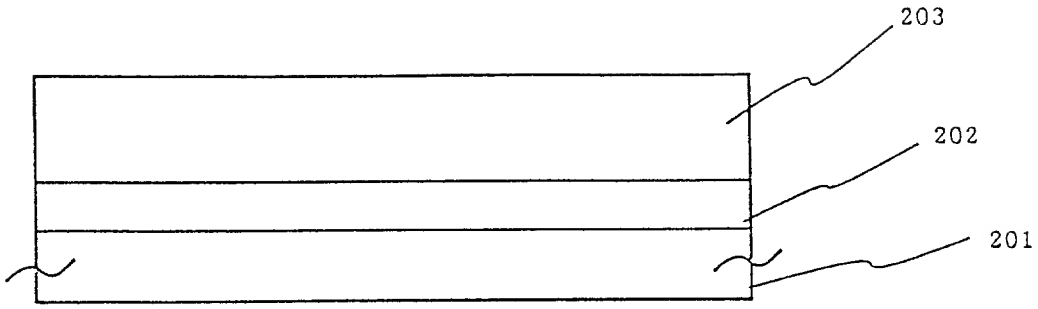


Fig. 2 (A)

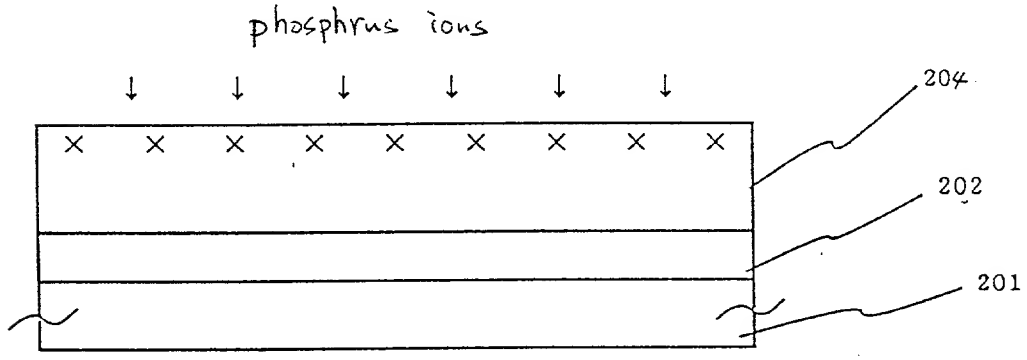


Fig. 2 (B)

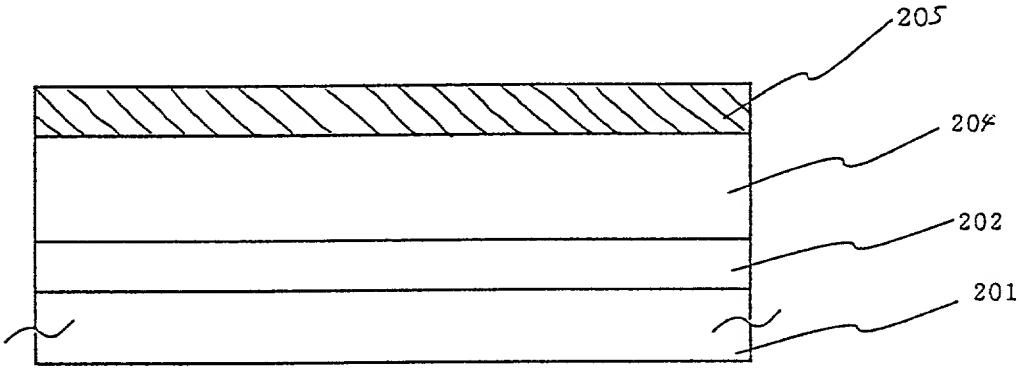


Fig. 2 (C)

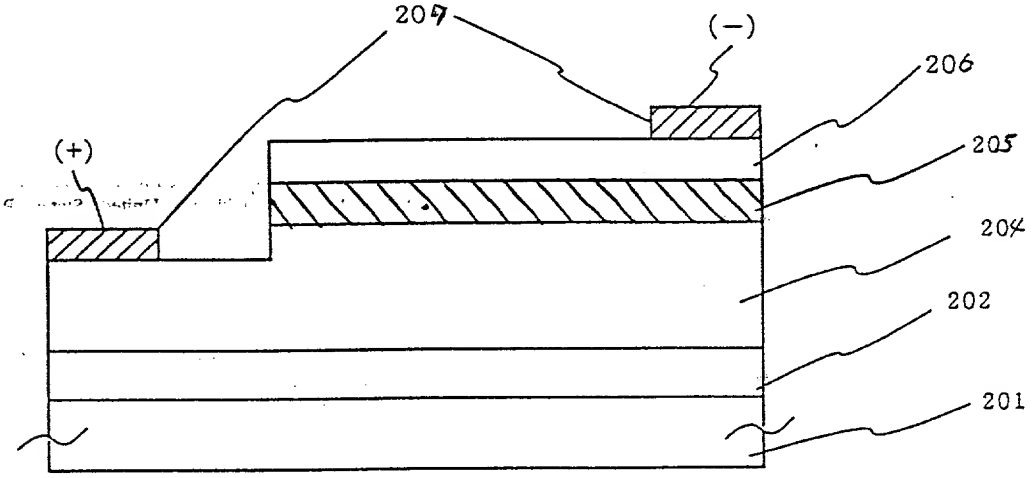


Fig. 2 (D)

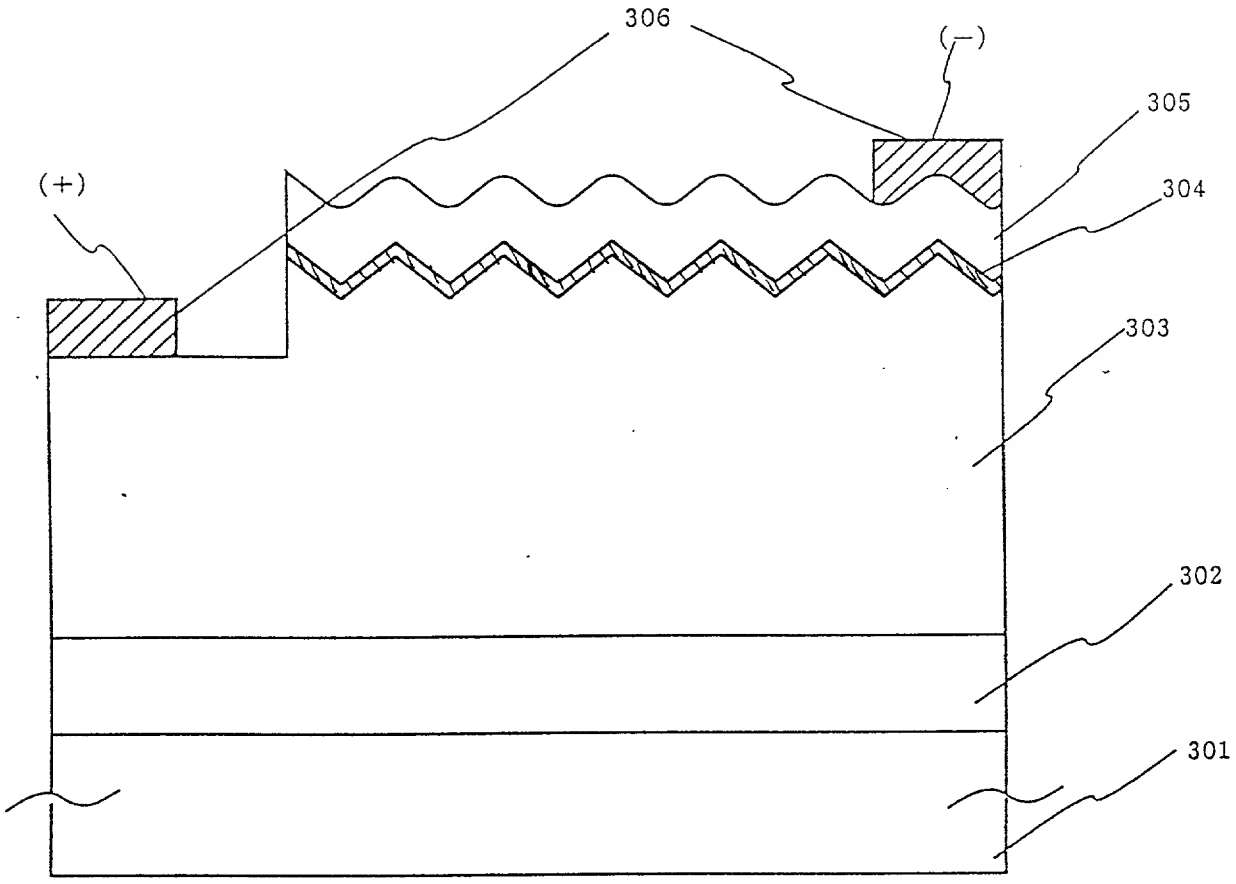


Fig. 3

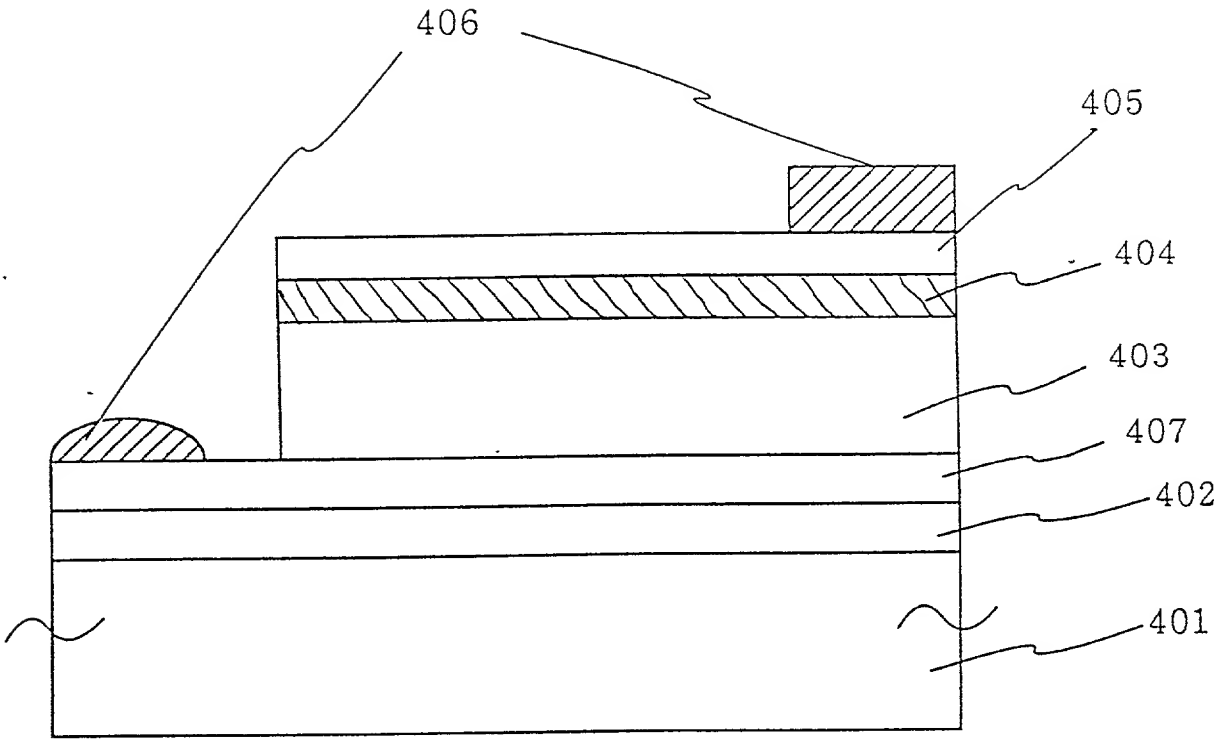


Fig. 4

Fig. 1A

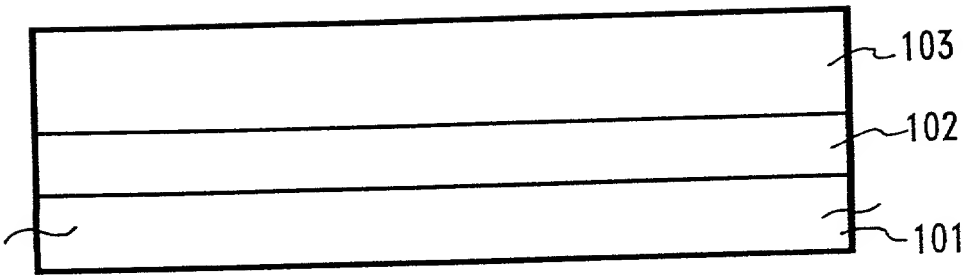


Fig. 1B

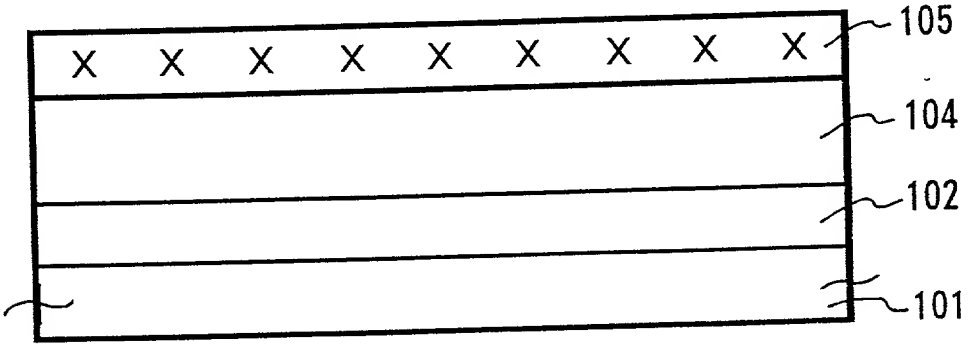


Fig. 1C

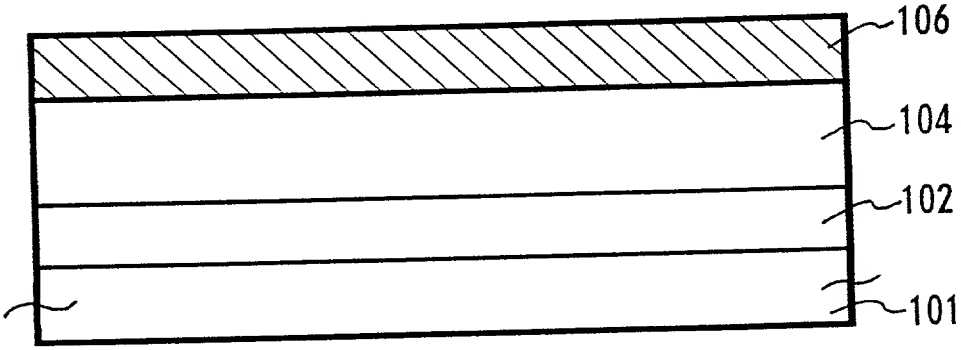


Fig. 1D

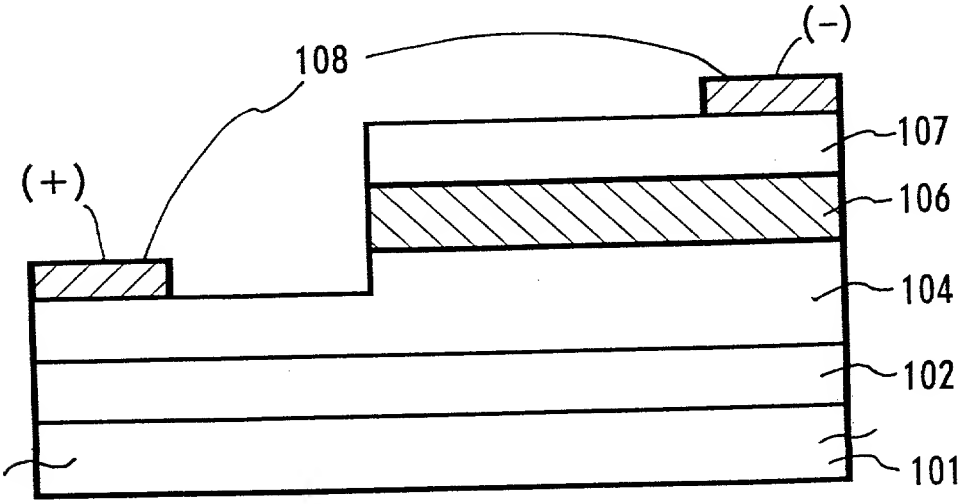


Fig. 2A

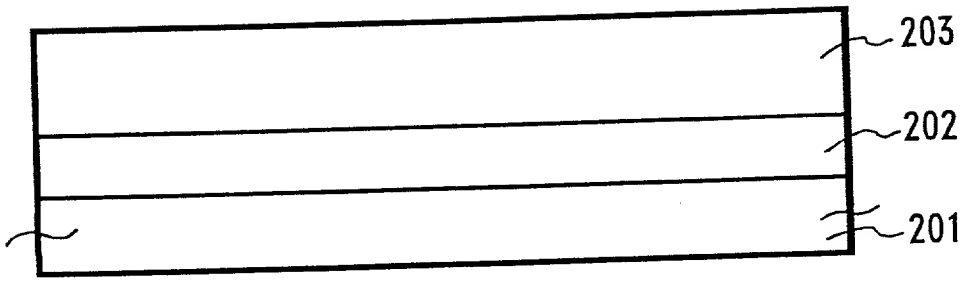


Fig. 2B

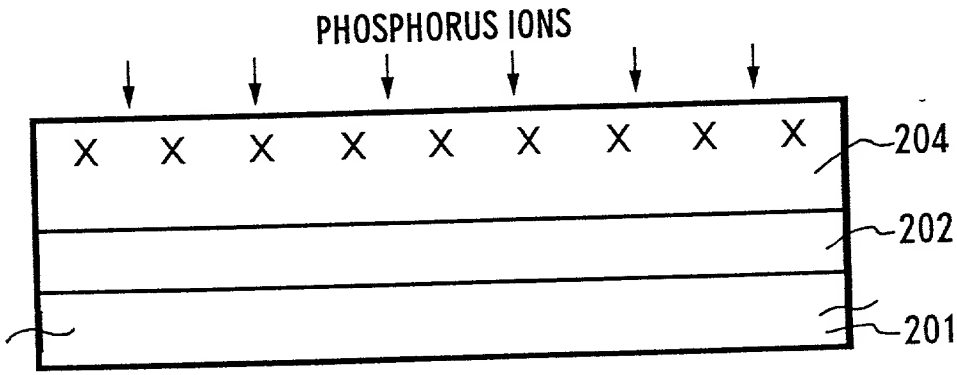


Fig. 2C

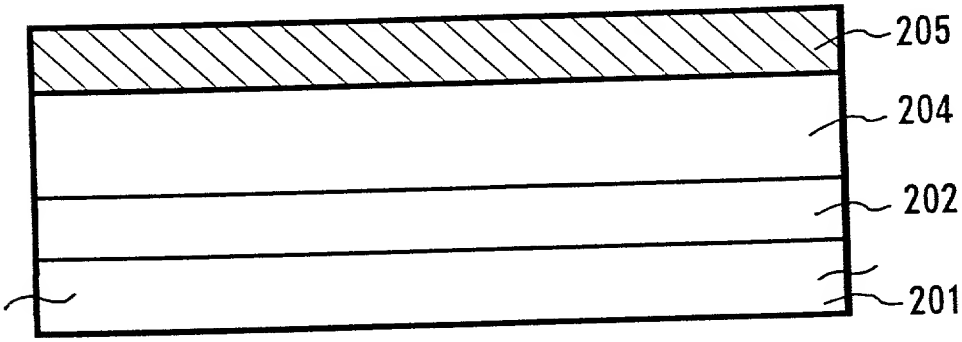
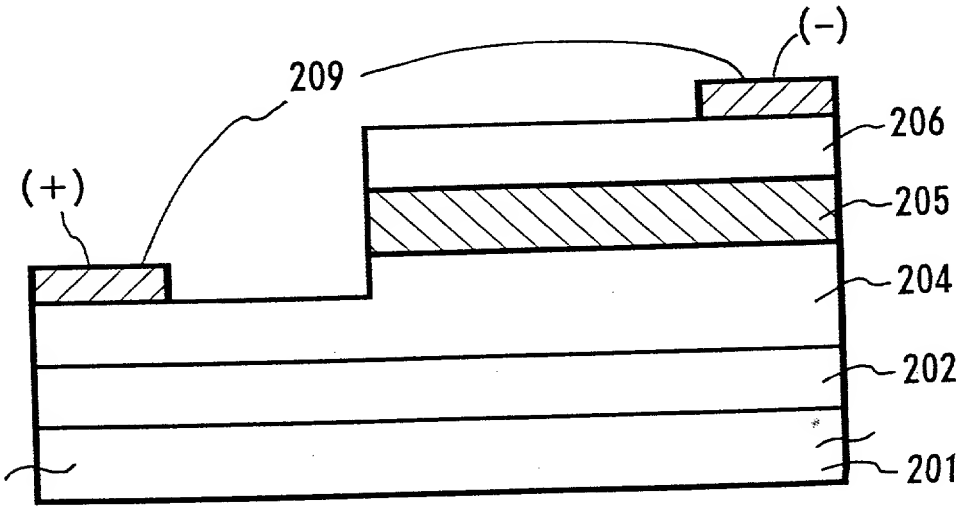


Fig. 2D



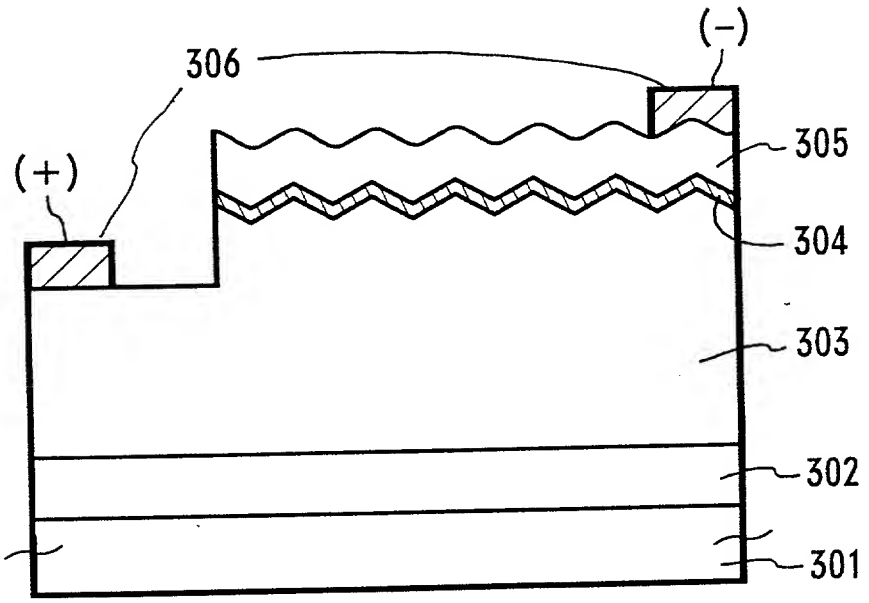


Fig. 3

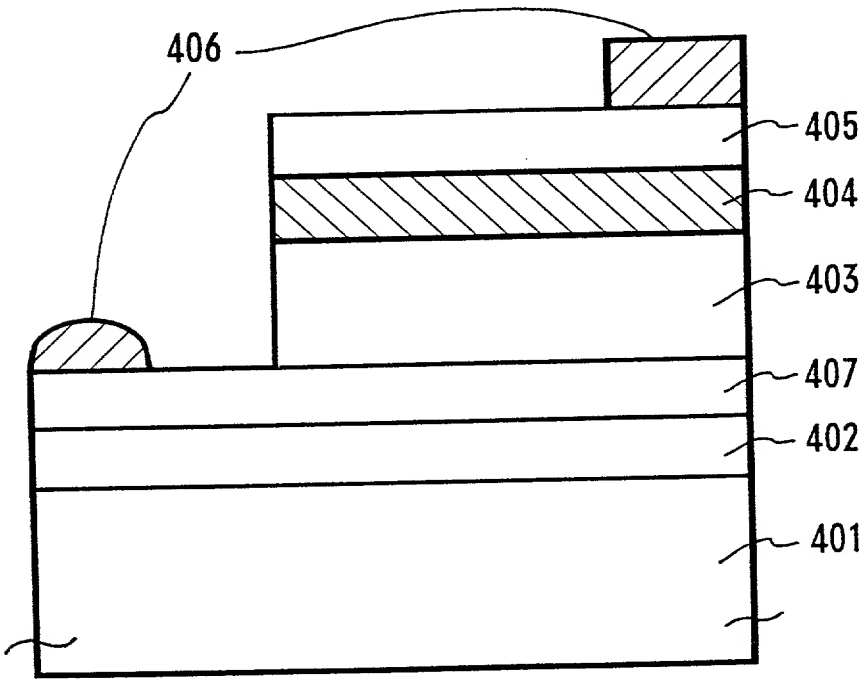


Fig. 4

PATENT
ATTORNEY DOCKET NO: 07977/023001

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

THIN-FILM PHOTOELECTRIC CONVERSION DEVICE AND A METHOD OF MANUFACTURING THE SAME

the specification of which

■ is attached hereto.

☐ was filed on _____ as Application Serial No. _____

and was amended on _____.

☐ was described and claimed in PCT International Application No. _____

filed on _____ and as amended under PCT Article 19 on _____.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information I know to be material to patentability in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate or of any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed:

COUNTRY	APPLICATION NO.	FILING DATE	PRIORITY CLAIMED
JAPAN	7-129865	March 27, 1995	☒ Yes ■ No
JAPAN	7-129864	March 27, 1995	☒ Yes ■ No
JAPAN	7-110121	April 11, 1995	☒ Yes ■ No
			☐ Yes ■ No

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patents issued thereon.

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